Appendix A

DDR DIB for Memory Tester

Purpose

This document describes specific requirements for any DDR DIB developed to provide an interface between bT72-332D memory tester developed by Acuid Corporation, and specific DDR DUT.

1 SCOPE

The scope of this document is the detailed set of requirements any DDR DIB should meet to be compatible with bT72-332D memory tester as well as with a specific DDR DUT.

2 DEFINITIONS

A, ADDR – DUT address signal.

BA – DUT bank select signal.

CAS - column address strobe signal in DUT.

CB – DUT check bit signal.

CK – DUT clock signal.

CKE - DUT clock enable signal.

CL - CAS latency, the number of clocks between the clock on which a Read command is issued and the clock on which read data appear on the DUT output.

DDR - double data rate, a technology used in synchronous dynamic memory modules which allows transferring data words at every edge of the clock signal.

DIB – DUT interface board, an electronic device (PCB-based normally) providing electronic and programming interface between a memory tester and a DUT.

DIB input connector – DIB connector interfacing header, which receives DUT driving signals, among others.

DIB output connector - DIB connector interfacing header, which sends signals from DUT to header, among others.

DIB unit – DIB complete with mechanical interfaces, chassis, accessories etc.

DIMM - dual-in-line memory module.

DLL - delay locked loop, a block used in DDR chips to compensate for temperature and voltage variations.

DM, DQMB – DUT low data mask signal.

DQ – input/output signal in DUT.

DQM - input/output mask signal in DUT. DQM is an input mask signal for write accesses and an output enable signal for read accesses.

DQS –low data strobe signal in DUT.

DRV – driver.

DUT - device under test.

ESD - electrostatic discharge.

Fault - an error occurring in the memory functional test. The following fault types are defined:

AF - address decoder fault.

CF - coupling fault. A write operation, which generates a transition in one cell, changes the content of a second cell (see ref 1, p.50).

CFid - idempotent coupling fault. A transition in one cell forces the content of a second cell to a certain value, 0 or 1 (see ref 1, p.51).

CFin - inversion coupling fault. A transition in one cell inverts the content of a second cell (see ref 1, p.50).

NPSF - neighborhood pattern sensitive fault. The content of a cell is influenced by the contents of surrounding cells in the memory (see ref 1, p.54).

SAF - stuck-at fault. A constant value of 0 or 1 in a cell output. SAF0 / SAF1 mean stuck-at-zero / stuck-at-one faults respectively.

TF - transition fault. It is a special case of the SAF. An up transition fault is defined as a fail to undergo a 0 to 1 transition in a write operation. A down transition fault is a failure to undergo a 1 to 0 transition on a write operation (see ref 1, p.47).

Unlinked fault - A fault is unlinked if it does not influence the behaviour of other faults (see ref 1, p.70).

FETEN – external control signal for DUT which has FET switches in DQ path.

FIFO - first input, first output, the definition of the queue behaviour which can be implemented as either a hardware block or software function

FPG - functional pattern generator, a bT module generating a data inversion signal as a function of the row and column addresses.

Handler – any mechanical means used to place/remove DUT in testing position, among other operations with DUT. Could be automated, semiautomated or manual.

Header – replaceable part of a memory tester providing interface for testing DUTs of specific types (DDR header, SDRAM header etc).

Heater – any means used to provide thermal environment for DUT in accordance with test procedure.

NRS – non-regular signal.

PMU – parametric unit, part of tester responsible for parametric measurements.

RAS - row address strobe signal in DUT.

RCD, tRCD - RAS to CAS delay timing parameter. RCD is used to express the parameter value in clocks, tRCD is used to express the value in nanoseconds.

RCV – receiver.

RP, tRP - RAS to precharge time. It is the time after the Precharge command and before the bank(s) will be available for subsequent row accesses. RP is used to express the parameter value in clocks, tRP is used to express the value in nanoseconds.

S – DUT chip select signal.

SA –SPD address signal.

SCL –SPD clock signal.

SDA –SPD data signal.

SDR - single data rate, opposite to DDR defined above in this section.

SDRAM - synchronous dynamic random access memory.

SGRAM - synchronous graphic random access memory.

SMD – surface mount device.

SPD - serial presence detect, an additional memory on memory module (DIB) to store information about the module (DIB) parameters.

TPL - test program language, the language in which tests are written.

VDD –voltage to power DUT input buffers and core logic.

VDDID – signal identifying whether VDD is separated from VDDQ.

VDDQ – voltage to power DUT output buffers.

VREF –reference voltage for SSTL2 inputs.

VT – termination voltage.

WE – DUT write strobe signal.

WP –write protect signal.

3 SPECIFICATION

3.1 Electrical

Electrically DIB has a basic purpose of providing an interface between header and a specific DUT. However, there could be additional purposes, such as providing interface to handler, heater etc. DUT types may vary widely. These could be most types of memory devices (not limited to DDR and SDR) as well as non-memory ones.

Depending on the DUT type, DIB can have a single as well as multiple DUT connectors (single-site and multi-site DIB).

Normally, each DUT type requires a unique DIB. However, some DUT types can be compatible enough to use a common DIB.

On the other hand, different DIBs may be needed for the same DUT. Such DIBs can differ electrically as well as by PCB layout. This depends on DUT connector type used, DUT handler requirements, heater requirements etc.

For any specific DUT, electrically different DIBs can be developed using a certain freedom of connecting DIB inputs and outputs to DUT. This freedom, as well as some essential connections, is described by assignments and rules outlined below.

In order to facilitate these rules all high-speed DUT signals are grouped by their functionality into two sets of groups in accordance with Table 1. Each signal can belong to only one of DRV and only one of RCV functional groups.

DQ RCV functional group encompasses all signals having "CB", "DQ" or "DQS" in their names (see Table 1). This means functionally combined signals (such as DM/DQS, for example) apply as well. Signals which do not fit the criteria for DQ RCV functional group comprise Control RCV functional group.[1]

[1] Please note there could be a DUT which signals cannot satisfy this specification. Such is the case when DUT has at least one pair of signals, one of which is functionally combined with DQS and another has the same functionality minus DQS (for example, DM/DQS and DM). In this case it is recommended to contact Acuid Corporation Ltd. for a solution.

High-speed DUT signal	DRV functional groups							RCV functional groups	
	DQ DRV	DQS DRV	Address DRV	DM DRV	Clock DRV	Select DRV	Control DRV	DQ RCV	Control RCV
A#			+						+
BA#			+						+
CAS_N							+		+
CB#	+							+	
CK#(_N)					+				+
CKE#							+		+
DM#				+					+
DQ#	+							+	
DQMB#				+					+
DQS#		+						+	
FETEN							+		+
RAS_N							+		+
S#_N						+			+
WE_N							+		+

Table 1: Groups of high-speed DUT signals

For a single-site DIB, when DUT is a DDR memory device, high-speed signals should be linked from DUT connector to header-interfacing connectors in a way shown in Figure 1. For SDR memory device the schematic should be as shown in Figure 2. Signal names correspond to pin assignments in Table 4 and Table 5.

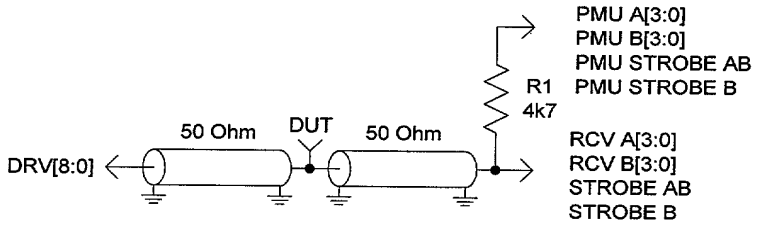


Figure 1: High speed signal schematic for DDR DUT

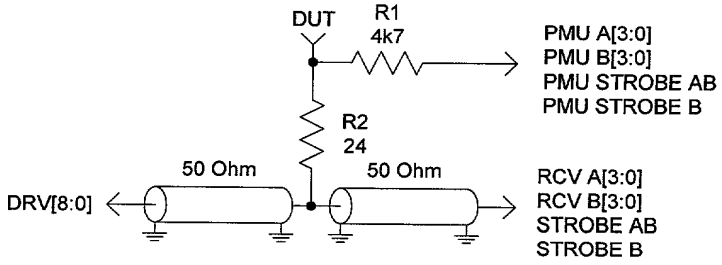


Figure 2: High speed signal schematic for SDR DUT

For a multi-site DIB, some of the high-speed signals may need to go to n DUTs (more than one). Whenever this is the case, signal schematic should be in accordance with Figure 3, both for DDR and SDR DUTs.

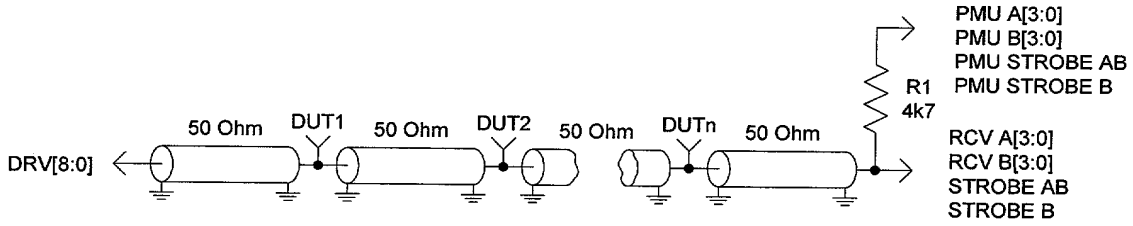


Figure 3: High speed signal schematic for signals common between multiple DDR DUTs

It is important that R1 and R2 resistors shown in Figure 1, Figure 2 and Figure 3 should have size no bigger than SMD0603 type.

Devices other than DDR or SDR memory could require different schematics. Some other issues could arise as well- it is recommended to contact Acuid Corporation Ltd. for a feasibility check in such case.

DIB should have 30 header-interfacing connectors 4x25=100 signal pins each. These connectors should be male, Z-Pack Stripline 100 type (AMP), or compatible. AMP product code is 646245-2. Connectors should be arranged as shown in Figure 4.

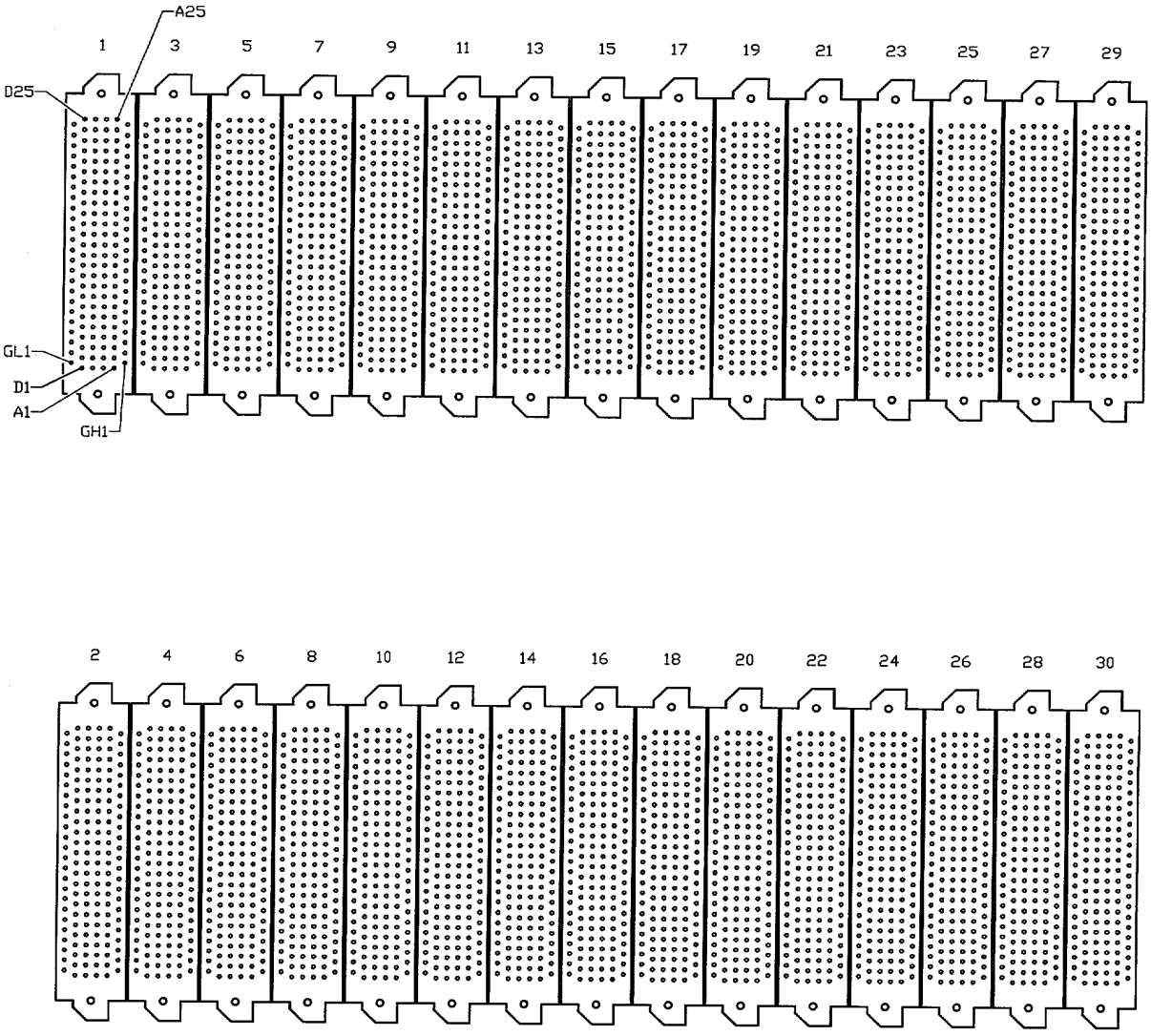


Figure 4: Header-interfacing connectors of DIB (viewed from mount side)

3.1.1 DIB header-interfacing connectors' assignments

Each header-interfacing connector can be assigned to only one of functional groups of signals assembled in accordance with Table 1.

	Connector #	1	3	5	7	9	11	13	15	17	19	21	13	25	27	29
Functional Group Name	DQ DRV	+		+	+		+	+			+		+		+	+
	DQS DRV	+		+	+		+	+	+		+		+		+	+
	Address DRV		+			+										
	DM DRV								+							
	Clock DRV									+						
	Select DRV													+		
	Control DRV											+				

Table 2: DRV functional group- connector assignments

	Connector #	2	4	6	8	10	12	14	16	18	20	22	24	26	28	30
Functional Group Name	DQ RCV	+		+	+		+	+			+		+		+	+
	Control RCV		+			+			+	+		+		+		

Table 3: RCV functional group- connector assignments

Please note that odd-numbered connectors (see Table 2) are intended to connect DIB to header output signals, whereas even-numbered ones (see Table 3)- to header input signals. However, DRV and RCV functional groups incorporate parts of the same set of DUT signals (such as DQ, DQS, DM, ADDR, BA etc.), albeit differently grouped. DUT signals are meant in wider sense here: these are either original DUT signals, or signals separated from DUT with an impedance-matching resistor R2, depending on the DUT type.

3.1.2 DIB header-interfacing connectors: pin assignments

Table 4 and Table 5 specify pin assignments in general. This means that every signal name marked with * specifies functionality of the pin it is assigned to, rather than unique signal name. This is clearly seen in Figure 1 and Figure 2. Thus, only GND signal can be considered ultimately assigned within Table 4 and Table 5. All other signals should be assigned in accordance with rules described below. After all necessary assignments are made, pins which do not acquire any signal should be left non-connected.

GH and GL pins (could be seen in Figure 4) are not listed in Table 4 and Table 5 for clarity. These pins should be connected to GND net.

Pin #	Assignment	Pin #	Assignment	Pin #	Assignment	Pin #	Assignment
A1	GND	B1	GND	C1	GND	D1	RELAY RESERVE*
A2	GND	B2	GND	C2	GND	D2	GND
A3	GND	B3	GND	C3	GND	D3	GND
A4	GND	B4	GND	C4	GND	D4	GND
A5	GND	B5	GND	C5	GND	D5	GND
A6	GND	B6	GND	C6	GND	D6	GND
A7	GND	B7	GND	C7	GND	D7	VT RCV A0*
A8	GND	B8	DRV0*	C8	GND	D8	GND
A9	GND	B9	GND	C9	VT DRV012*	D9	VT RCV A1*
A10	GND	B10	DRV1*	C10	GND	D10	GND
A11	GND	B11	GND	C11	VT DRV012*	D11	VT RCV A2*
A12	GND	B12	DRV2*	C12	GND	D12	GND
A13	GND	B13	GND	C13	VT DRV012*	D13	VT RCV A3*
A14	GND	B14	DRV3*	C14	GND	D14	GND
A15	GND	B15	GND	C15	VT DRV345*	D15	VT STROBE AB*
A16	GND	B16	DRV4*	C16	GND	D16	GND
A17	GND	B17	GND	C17	VT DRV345*	D17	VT RCV B0*
A18	GND	B18	DRV5*	C18	GND	D18	GND
A19	GND	B19	GND	C19	VT DRV345*	D19	VT RCV B1*
A20	GND	B20	DRV6*	C20	GND	D20	GND
A21	GND	B21	GND	C21	VT DRV678*	D21	VT RCV B2*
A22	GND	B22	DRV7*	C22	GND	D22	GND
A23	GND	B23	GND	C23	VT DRV678*	D23	VT RCV B3*
A24	GND	B24	DRV8*	C24	GND	D24	GND
A25	GND	B25	GND	C25	VT DRV678*	D25	VT STROBE B*

Table 4: Pin assignments for odd-numbered connectors

Pin #	Assignment	Pin #	Assignment	Pin #	Assignment	Pin #	Assignment
A1	GND	B1	GND	C1	GND	D1	GND
A2	GND	B2	RCV A0*	C2	GND	D2	PMU A0*
A3	GND	B3	GND	C3	GND	D3	GND
A4	GND	B4	RCV A1*	C4	GND	D4	PMU A1*
A5	GND	B5	GND	C5	GND	D5	GND
A6	GND	B6	RCV A2*	C6	GND	D6	PMU A2*
A7	GND	B7	GND	C7	GND	D7	GND
A8	GND	B8	RCV A3*	C8	GND	D8	PMU A3*
A9	GND	B9	GND	C9	GND	D9	GND
A10	GND	B10	STROBE AB*	C10	GND	D10	PMU STROBE AB*
A11	GND	B11	GND	C11	GND	D11	GND
A12	GND	B12	RCV B0*	C12	GND	D12	PMU B0*
A13	GND	B13	GND	C13	GND	D13	GND
A14	GND	B14	RCV B1*	C14	GND	D14	PMU B1*
A15	GND	B15	GND	C15	GND	D15	GND
A16	GND	B16	RCV B2*	C16	GND	D16	PMU B2*
A17	GND	B17	GND	C17	GND	D17	GND
A18	GND	B18	RCV B3*	C18	GND	D18	PMU B3*
A19	GND	B19	GND	C19	GND	D19	GND
A20	GND	B20	STROBE B*	C20	GND	D20	PMU STROBE B*
A21	GND	B21	GND	C21	GND	D21	GND
A22	NRS0*	B22	NRS1*	C22	NRS2*	D22	NRS3*
A23	NRS4*	B23	NRS5*	C23	NRS6*	D23	NRS7*
A24	NRS8*	B24	NRS9*	C24	NRS10*	D24	NRS11*
A25	NRS12*	B25	NRS13*	C25	NRS14*	D25	NRS15*

Table 5: Pin assignments for even-numbered connectors

Pins DRV0 - DRV8 (see Table 4) can belong to any functional group of signals listed in Table 2.

Signals from DQ DRV, DQS DRV, DM DRV, Clock DRV, Select DRV and Control DRV functional groups can be assigned freely within respectively designated connectors. This means any signal from mentioned groups could be assigned to any specified pin within connector(s) designated for respective group.

For Address DRV functional group some limitations apply. Signals ADDR0 - ADDR4, ADDR6, ADDR10, BA0, BA1 should be assigned to connector #9, and signals ADDR5, ADDR7 - ADDR9, ADDR11 - ADDR14, BA2 - to connector #3. Within specified pins of the named connectors, the order of signals is free.

Unlike other functional groups, DQ RCV group is a structured one. Its DQ signals are grouped with DQS signals in accordance with DUT specification. This means DQ RCV group consists of DQS RCV subgroups having one DQS and some associated DQ signals each (4 or 8 DQ signals normally). DQS signals may be functionally combined ones, like DM/DQS.

Consequently, each connector assigned to the DQ RCV functional group should be dedicated to one or two above named DQS RCV subgroups, depending on their size. Subgroups can be assigned to specified connectors in a free order, i.e. any subgroup(s) to any connector assigned to DQ RCV group.

Within a connector, a certain order of assigning signals from a DQS RCV subgroup to specified pins should be followed.

If a subgroup has no more than 4 DQ signals, it can be assigned to the connector in three ways. One is to assign DQ signals to RCV A0 - RCV A3 pins, with DQS signal assigned to STROBE AB pin. Another one is to assign DQ signals to RCV B0 - RCV B3 pins, with DQS signal assigned to STROBE B pin. Third way is to assign DQ signals to RCV A0 - RCV A3 and RCV B0 - RCV B3 pins, with DQS signal assigned to STROBE AB (not STROBE B!) pin. The last way is the only possible one when a subgroup has 5-8 DQ signals. Within a DQS RCV subgroup DQ signals can be assigned to specified pins in a free order in any case.

Signals from Control RCV functional group can be assigned in free order to RCV A0 - RCV A3 and RCV B0 - RCV B3 pins of specified connectors (Table 3). The only exceptions are CK#(_N) signals (Table 1). These could be assigned to any pin of the same connectors, including STROBE AB and STROBE B pins, with the latter being preferred for CK#(_N) signals.

As a result of all said above and having in mind Figure 1 or Figure 2, Table 4 and Table 5, signals from any odd-numbered header-interfacing connector should go to DUT connector and then to an even-numbered connector. DUT may be connected directly, or by an impedance-matching resistor R2. Importantly, the named two connectors can belong to different columns as well as the same one.

All the above rules describe the freedom to connect DUT signals. This freedom is needed to make connections allowing simpler PCB, to easier meet PCB design and layout rules, as well as any other requirements.

VT DRV012, VT DRV345 and VT DRV678 pins should be connected to VT RCV A0 - VT RCV A3, VT RCV B0 – VT RCV B3, VT STROBE AB and VT STROBE B pins (Table 4) using the following instructions.

- Whenever a pin DRV# (one of DRV0- DRV8) of an odd-numbered connector is linked to a pin of an even-numbered connector (net A), a correlated link should be provided (net VT A). This link should connect two pins as minimum.
- One pin of net VT A belongs to VT DRV012, VT DRV345 and VT DRV678 set of the same connector as DRV# pin of net A, any of three digits in its name matching the one in DRV# name. Examples: VT DRV345 and DRV5, VT DRV678 and DRV7.
- Another pin of net VT A belongs to VT RCV A0 - VT RCV A3, VT RCV B0 – VT RCV B3, VT STROBE AB, VT STROBE B set of an odd-numbered connector that is located in the same column as an even-numbered one which has net A connected. This pin should have a name matching that of the even-numbered connector's pin, net A. Examples: VT RCV A2 and RCV A2, VT STROBE B and STROBE B (see Table 4 and Table 5).

Taking into account that each of VT DRV012, VT DRV345 and VT DRV678 pins is duplicated three times within an odd-numbered connector, duplicated pins could be connected together, or only one of duplicated pins used in relation to DRV0, DRV1, DRV2, or DRV3, DRV4, DRV5, or DRV6, DRV7, DRV8 pins. In these cases VT A net would connect together up to 6 pins.

PMU A0- PMU A3, PMU B0- PMU B3, PMU STROBE AB and PMU STROBE B pins should be connected in accordance with Figure 1 or Figure 2. The rules are as follows.

Any signal pin of the DUT connector should be linked to two pins of a single even-numbered connector (one by R1, another directly or by R2). These pins should have matching names. Examples: PMU A1 and RCV A1, PMU STROBE AB and STROBE AB.

RELAY RESERVE pins of odd-numbered connectors (see Table 4) could be used for driving relays or similar use on DIB or DIB-attached devices if needed.[2]

NRS0 – NRS15 pins could be assigned to various signals in accordance with Table 6.

[2] Present version of software does not support usage of these pins- please contact Acuid Corporation Ltd. if you have a need to use them.

CONNECTOR #		2	4	6	8	10	12	14	16	18
NRS#	NRS0	"RUN" BUTTON (note 1)	VDD (note 2)	n.c.	n.c.	VDDQ (note 2)	n.c.	PMU SENSE RESERVE1 (note 3)	RESET N (note 2)	WP
	NRS1	n.c.	VDD	n.c.	n.c.	VDDQ	n.c.	PMU SENSE RESERVE2 (note 3)	VDDID (note 2)	SA2
	NRS2	GND (note 2)	VDD	n.c.	n.c.	VDDQ	n.c.	PMU SENSE RESERVE3 (note 3)	VREF (note 2)	SA1
	NRS3	GND (note 2)	VDD	n.c.	n.c.	VDDQ	n.c.	PMU SENSE RESERVE4 (note 3)	n.c.	SA0
	NRS4	n.c.	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	RESET N (note 2)	WP SENSE
	NRS5	n.c.	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	VDDID (note 2)	SA2 SENSE
	NRS6	GND (note 2)	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	VREF (note 2)	SA1 SENSE
	NRS7	GND (note 2)	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	n.c.	SA0 SENSE
	NRS8	n.c.	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	n.c.	SDA
	NRS9	n.c.	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	n.c.	SCL
	NRS10	GND (note 2)	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	n.c.	VDDSPD (note 2)
	NRS11	GND (note 2)	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	n.c.	n.c.
	NRS12	n.c.	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	n.c.	SDA SENSE
	NRS13	n.c.	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	n.c.	SCL SENSE
	NRS14	GND (note 2)	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	n.c.	VDDSPD (note 2)
	NRS15	GND (note 2)	VDD	n.c.	n.c.	VDDQ	n.c.	n.c.	n.c.	Do not connect

Notes:

1. Connecting this pin to GND net with a button switch (normally open) or other means generates "RUN" command
2. Special routing rules apply to this pin
3. Present version of software does not support usage of this pin- please contact Acuid Corporation Ltd. if you have a need to use it.

Table 6 : NRS signal assignments

CONNECTOR #		20	22	24	26	28	30
NRS#	NRS0	RETURN +5(+15)	DIB FEEDBACK1 (note 3)	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS1	RETURN +5(+15)	DIB FEEDBACK2 (note 3)	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS2	RETURN +5(+15)	DIB FEEDBACK3 (note 3)	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS3	RETURN +5(+15)	DIB FEEDBACK4 (note 3)	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS4	RETURN +5(+15)	DIB RELAY1 N (note 3)	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS5	RETURN +5(+15)	DIB RELAY2 N (note 3)	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS6	RETURN +5(+15)	DIB RELAY3 N (note 3)	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS7	RETURN +5(+15)	n.c.	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS8	RETURN +5(+15)	n.c.	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS9	RETURN +5(+15)	n.c.	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS10	RETURN +5(+15)	n.c.	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS11	RETURN +5(+15)	n.c.	Do not connect	n.c.	+5V (note 5)	+15V (note 6)
	NRS12	RETURN +5(+15)	n.c.	DIB SDA	"BUSY" LED (note 4)	+5V (note 5)	+15V (note 6)
	NRS13	RETURN +5(+15)	n.c.	DIB SCL	"FAIL" LED (note 4)	+5V (note 5)	+15V (note 6)
	NRS14	RETURN +5(+15)	n.c.	DIB WP	"PASS" LED (note 4)	+5V (note 5)	+15V (note 6)
	NRS15	RETURN +5(+15)	n.c.	VDD DIB SPD	"POWER" LED (note 4)	+5V (note 5)	+15V (note 6)

Notes:

3. Present version of software does not support usage of this pin- please contact Acuid Corporation Ltd. if you have a need to use it.

4. Using this pin requires some hardware changes in DDR header- please contact Acuid Corporation Ltd. if you have a need to use it.

5. Maximum power consumption for +5V is 1A

6. Maximum power consumption for +15V is 1A

Table 5 (continued): NRS signal assignments

NRS0- NRS9, NRS12 and NRS13 pins of connector #18 (see Table 6) should be connected in accordance with Figure 5.

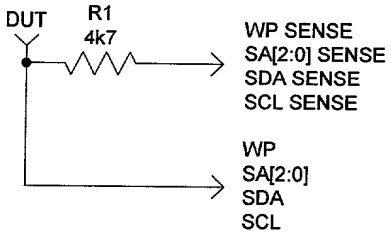


Figure 5: DIB- slow speed signal schematic

NRS12- NRS15 pins of connector #24 (see Table 6) should be connected to SPD chip on DIB in accordance with Figure 6.

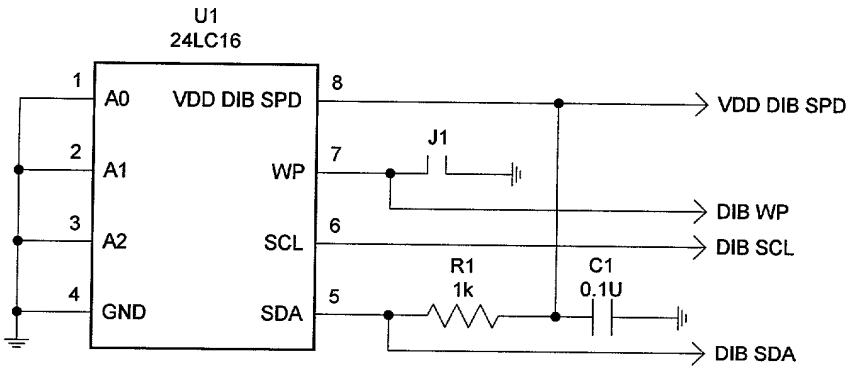


Figure 6: DIB- SPD schematic

3.2 PCB design

PCB design and layout of DIB should follow some rules described below.

Any signal from any functional group listed in Table 2 and Table 3 should be routed with traces with matched impedance of 50±5 Ohm (see Figure 1 and Figure 2). Impedance should be measured at 1GHz or by TDR method with 400ps signal edge.

Cross talk between any pair of traces, with at least one having matched impedance, should not exceed –60dB.

An example of a matched impedance layer configuration providing for the above requirements is shown in Figure 7, with an example of DIB PCB build shown in Table 7.

However, such impedance precision is not enough to provide signal skew within spec. Certain groups of traces should have smaller impedance difference. Since making tight manufacturing tolerances is normally not possible to desired levels, it is necessary to use a rule for assigning signals to PCB layers. This rule applies to any functional group listed in Table 2 and Table 3 except Control RCV group.

The rule is: signals assigned to a single header-interfacing connector and belonging to any one of functional groups mentioned above should be routed within a single layer along a stretch from that connector to DUT connector. Taking into account that each signal has two such stretches (see Figure 1 and Figure 2), it can be routed within two different layers (one for each stretch), as well as within a single layer.

In case DUT connector is separated from matched impedance routes with impedance-matching resistors R2 (Figure 2), routes between these resistors and DUT connector should be short as possible (no longer than 2.54mm preferably). Non-impedance stubs of routes with matched impedance should be no longer than 1.53mm.

Resistor R1 featured in Figure 5 should have a link to DUT connector as short as possible.

Following rules apply to route lengths. The latter should be measured as propagation delays from pin of DUT connector to pin of header-interfacing connector.

Propagation delays in routes belonging to signals of any DRV functional group (listed in Table 2) should not differ more than 100ps between different header-interfacing connectors. The same applies separately to routes belonging to signals of RCV functional groups (listed in Table 3). This means that difference in propagation delays between DRV and RCV functional groups is not restricted.

Within each header-interfacing connector, propagation delays of routes should not differ more than 1ps. This applies to routes belonging to any functional group listed in Table 2 and Table 3, except Control RCV group.

Some rules apply to routing GND, VDD, VDDQ, RESET N, VDDID, VREF and VDDSPD nets.

GND should be routed with plane(s), except for some pins of header-interfacing connector #2 (see Table 6, note 1). Each of these pins should be connected to GND plane only with a route going to a single (any) pin of the DUT connector. The latter should be the same pin for every one of eight mentioned pins of connector #2 (NRS2, NRS3, NRS6, NRS7, NRS10, NRS11, NRS14 and NRS15).

VDD and VDDQ: each should be routed with a plane preferably. Otherwise these could be routed with split planes within the same layer. Pins NRS0 of connectors #4 and #10 are the exceptions here (see Table 6, note 1). Each of these pins should be connected to respective plane only with a route going to a single pin of the DUT connector. The latter pin should be the one most distant from NRS1- NRS15 pins of connector #4 or #10, respectively.

RESET N, VDDID, VREF and VDDSPD should be routed with a trace that goes from a header-interfacing connector to DUT connector and back to another pin of the same header-interfacing connector. Example: NRS2 - DUT connector - NRS6 (for VREF net, connector #16).

Mechanically, DIB PCB should meet all the requirements imposed by connectors used, mechanical design of the DIB unit, DUT heater, DUT handler etc. In case standard DIB unit design developed by Acuid Corporation Ltd is supposed to be used with a newly designed DIB PCB, the latter should be in accordance with Figure 8.

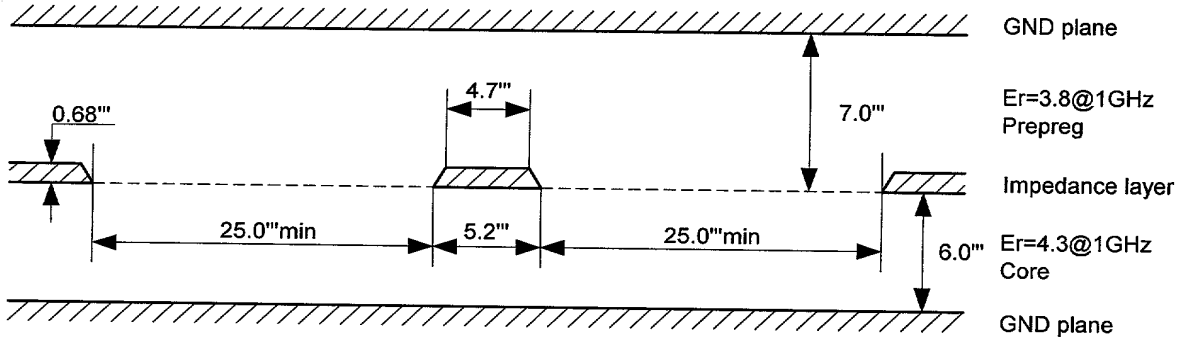
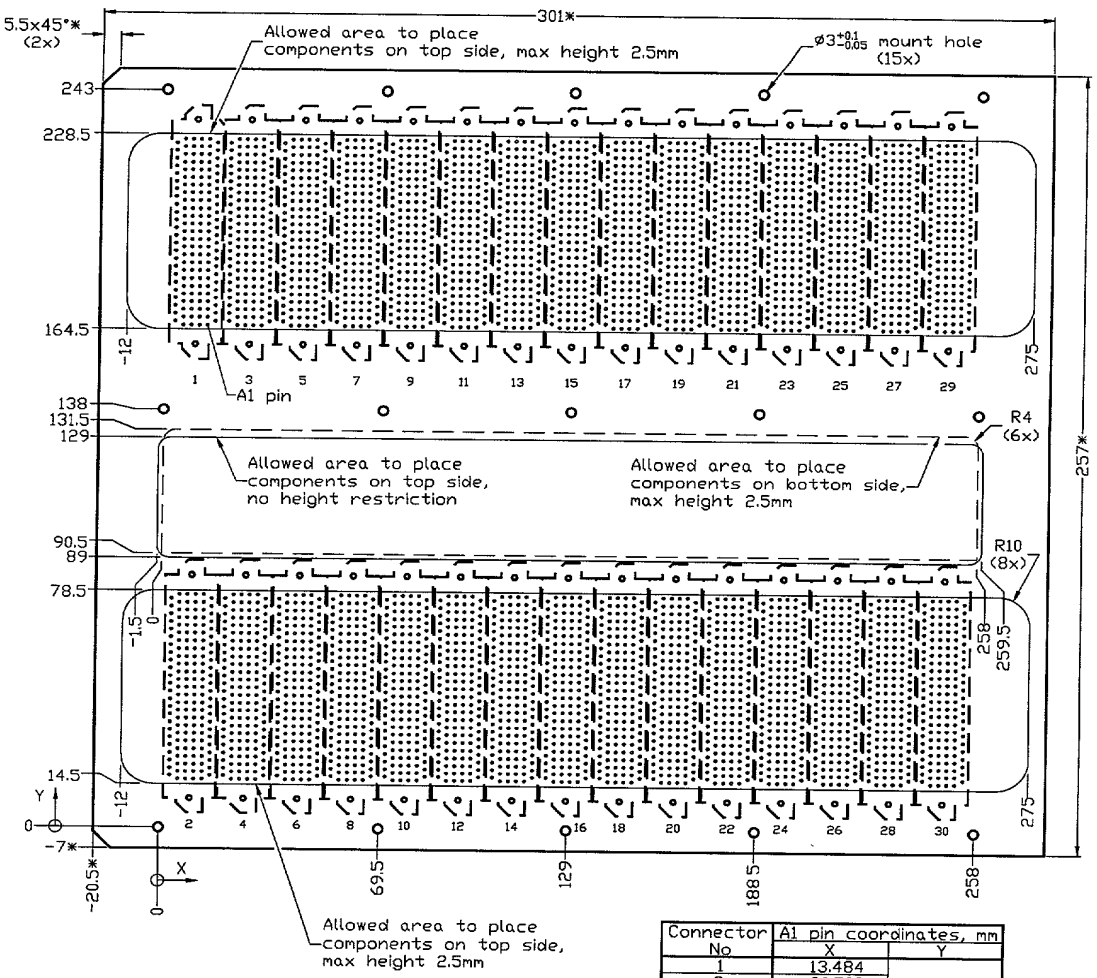


Figure 7: 50 Ohm matched impedance layer configuration (by Acuid Corporation Ltd.)

No	Layer type	Material	Dielectric constant	Thickness
1	L1, Top layer	Copper		0.5oz/0.68'"/17um
2	Prepreg	FR-4	3.8@1GHz	7'"/0.178mm
3	L2, Impedance traces	Copper		0.5oz/0.68'"/17um
4	Core	FR-4	4.3@1GHz	6'"/0.152mm
5	L3, Split/Mix. Plane	Copper		0.5oz/0.68'"/17um
6	Prepreg	FR-4	3.8@1GHz	7'"/0.178mm
7	L4, Impedance traces	Copper		0.5oz/0.68'"/17um
8	Core	FR-4	4.3@1GHz	6'"/0.152mm
9	L5, Split/Mix. Plane	Copper		0.5oz/0.68'"/17um
10	Prepreg	FR-4	3.8@1GHz	7'"/0.178mm
11	L6, Impedance traces	Copper		0.5oz/0.68'"/17um
12	Core	FR-4	4.3@1GHz	6'"/0.152mm
13	L7, Split/Mix. Plane	Copper		0.5oz/0.68'"/17um
14	Prepreg	FR-4	3.8@1GHz	7'"/0.178mm
15	L8, Impedance traces	Copper		0.5oz/0.68'"/17um
16	Core	FR-4	4.3@1GHz	6'"/0.152mm
17	L9, Split/Mix. Plane	Copper		0.5oz/0.68'"/17um
18	Prepreg	FR-4	3.8@1GHz	7'"/0.178mm
19	L10, Impedance traces	Copper		0.5oz/0.68'"/17um
20	Core	FR-4	4.3@1GHz	6'"/0.152mm
21	L11, Split/Mix. Plane	Copper		0.5oz/0.68'"/17um
22	Prepreg	FR-4	3.8@1GHz	7'"/0.178mm
23	L12, Impedance traces	Copper		0.5oz/0.68'"/17um
24	Core	FR-4	4.3@1GHz	6'"/0.152mm
25	L13, Split/Mix. Plane	Copper		0.5oz/0.68'"/17um
26	Prepreg	FR-4	3.8@1GHz	7'"/0.178mm
27	L14, Bottom layer	Copper		0.5oz/0.68'"/17um

Table 7: DIB PCB build developed by Acuid Corporation Ltd.



Connector No	A1 pin coordinates, mm	
	X	Y
1	13.484	165.823
3	30.502	
5	47.520	
7	64.538	
9	81.556	
11	98.574	
13	115.592	
15	132.610	
17	149.628	
19	166.646	
21	183.664	
23	200.682	
25	217.700	
27	234.718	
29	251.736	
2	13.484	16.217
4	30.502	
6	47.520	
8	64.538	
10	81.556	
12	98.574	
14	115.592	
16	132.610	
18	149.628	
20	166.646	
22	183.664	
24	200.682	
26	217.700	
28	234.718	
30	251.736	

Notes:
1. All dimensions are in millimeters unless otherwise stated
2. All position tolerances are ±0.05mm
3. Hole diameters for connector pins are dependent on connector type
4. * - specified PCB outline shows the maximum possible size, can be cut closer to ø3 mount holes if excessive
5. PCB thickness is 2.2mm

Figure 8: DIB PCB features required by standard DIB unit design (by Acuid Corp. Ltd.)

Appendix B

Fine Skew Adjustment Procedure for DDR Header

Equipment Required

1. A calibrated 1GHz bandwidth, 4GS/s sample rate digital oscilloscope, or better, with minimum of 2 active probes (including differential one) with no more than 1pF input capacitance.
2. Base board RevE (SYNBASEE) or RevD (SYNBASED) assembled in a Base case, set of 15 pincards DDRPEC1C or DDRPEC1D and Header board DDRHDRB,DDRHDRC or DDRHDRD assembled in a Header case.
3. DIB revision DDRDC1C.
4. DDRSCB card for skew measurement.
5. An appropriate hardware/software configured PC running Acuid Tools Software.

1 Procedure Algorithm

1. Run Calibration from Acuid Tools. It must finish successfully. If it doesn't, return Header to debugging.
2. On all fast DUT signals measure skew in respect to the reference clock signal (see section 3 for details) and save results.
3. If skew of signals is within the range of ±200ps then go to step 7, otherwise continue.
4. Update the correction factors stored in the Header's flash-memory. (See sections 4 for details on updating flash-memory).
5. Go to step 2.
6. Save Header SPD to a file (See sections 4 for details).

2 Individual Signal Skew Measurement

The skew of a signal is measured with respect to the reference differential clock signal CK0. Clock signal CK1 is used to trigger the scope. Note that for skew measurement all signals are observed on test points of DDRSCB card. Both rising and falling edges of the signal being measured are to be considered. To observe them simultaneously you need to configure the scope to accumulate waveforms with reasonable persistence and trigger from a clock signal.

Skew measurements are performed whilst the system is running the "Skew" test started under the Acuid Tools software. This test is running continuously and generates transitions on all signals to be checked.

To achieve the best possible precision and resolution the scope should have only one channel activated when taking measure. This will ensure that the total sample rate is not divided between several channels and all assigned to the channel of interest. The other channel is only used to trigger the scope.

There are four types of DDR DUT fast signals:

DDR signals such as DQ0 – DQ63, CB0 – CB7, DM0 – DM7;

SDR signals – A0 – A14, CKE0, CKE1, S0 – S4, RAS, CAS, WE, FETEN;

Clock signals – CK0, CK1, CK2;

DQS signals – DQS0 – DQS7.

DDR signals are sampled relative to both edges of clock. This entail that signal skew adjustment procedure involves two stages of measurement:

1. Skew measurement for all signals in respect to the rising edge of clock;
2. Skew measurement for DDR signals in respect to the falling edge of clock.

SDR signals are sampled relative to rising edge of clock therefore only the measurement on respect to the rising edge of clock is relevant.

CK1, CK2 are differential signals. Skew of these signals needs to be measured with differential probe in respect to rising and falling edges of clock signal CK0.

DQS signals repeat waveform of clock. Skew of DQS signals is measured in respect to rising and falling edges of clock.

For initial tuning enable the trigger channel connected to CK1 and adjust trigger level to 1.25V. Make sure you observe expected edge of the clock. Connect the other (differential) channel to CK0. This will be the reference signal for skew measurements. Then disable the first channel.

The skew is to be measured at 1.25V level. Therefore it is convenient to adjust the vertical position of the displayed signal so that the scope's central horizontal line corresponds to the 1.25V level. Enable vertical cursors to measure time intervals. Set the first cursor to the point where the center of the differential clock edge crosses the 0V level. Then select the second cursor so the first one remains stable in further measurements. The figure below illustrates how it should look like.

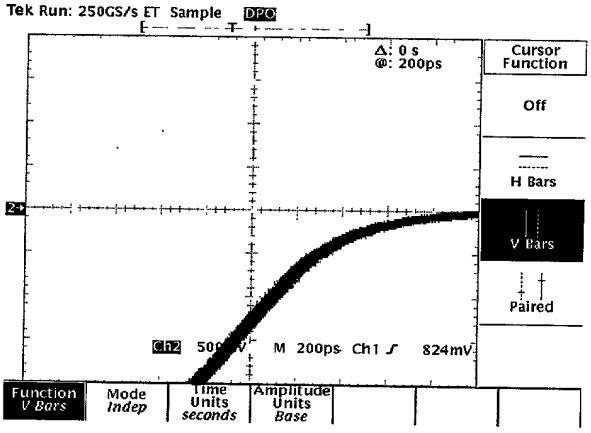
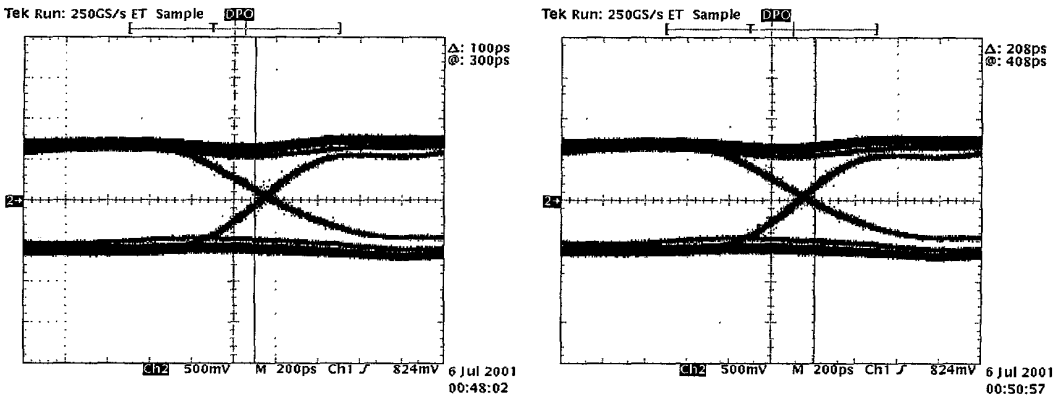


Fig.1. Reference clock signal CK0.

Disconnect the measuring probe from CK0 and connect to a signal requiring skew measurement. Using the second vertical cursor make two skew measurements on each signal left and right. The left skew is to be measured at the left-most point of signal traces crossing 1.25V level on the scope's screen. The right skew is to be measured at the right-most point of signal traces crossing 1.25V level on the scope's screen. The figures below illustrate how it should look like.



signal left skew = 100 ps signal right skew = 208 ps

Fig.2. Signal skew measurement.

The individual signal skew is a signed value. For points on the left of the first cursor (read: of the Clock edge) the skew has negative value. For points on the right of the first cursor the skew has positive value.

Repeat the above procedure of measurement to measure skew of DDR signals in reference to the falling edge of clock signal. For this measurement the scope trigger needs to be set at the falling edge, the trigger level remains the same 1.25 V.

Thus four measurements should be done for each DDR signal such as DQ, DM, CB – left and right skew in respect to the rising and falling edges of clock signal. Two measurements should be done for each SDR signal such as addresses A and controls CKE, RAS, CAS, WE, FETEN. These two measurements are left and right skew in respect to the rising edge of clock signal. Also two skew measurements should be done for DQS and clock signals. Note that skew of these signals is measured at the average point of signal traces crossing 1.25V level on the scope's screen.

Skew adjustment is an iterative process, so it is convenient to save results of skew measurements in a table. The table provided in the Appendix B could be an example of such table. Also the table provided in the DDR_Skew.xls file is suitable for storing the results of skew measurement.

3 Group Update

Each group of signals register has it's own Timing control means. Therefore skew can be adjusted for a group as a whole. The signals are grouped as provided in the "Typical Signal Grouping" table (see Appendix B for details). For each group only a signal with most left skew and a signal with most right skew need to be taken into account. The update to the propagation time for a given group is an additional delay value required to make the left maximum and the right maximum skew symmetrical in respect to the reference clock. It is calculated as follows:

$$\mathbf{UPDATE} = (T_{MIN} + T_{MAX})/2 \quad \text{(ps)}$$

where T_{MIN} is a minimum left skew value among of all the individual signal skews measured on signals of the given group;
T_{MAX} is a maximum right skew value among of all the individual signal skews measured on signals of the given group.

UPDATE values for groups have to be calculated for all iterations except the final one. To facilitate the work there is a special table in theDDR_Skew.xls file. The table contains skew records and **UPDATE** values calculated for each group. **UPDATE** values need to be added to the correspondent correction values in the on-DIB flash memory (see section 4 for details).

4 SPD reader/writer

The SPD Writer software tool is used to read, write and update contents of the on-DIB flash memory, otherwise known as Series Presence Detect memory (SPD). Do not confuse this memory with the Series Presence Detect chips on DIMMs. We hereafter describe using of the SPD Reader/Writer tool to update signal delays.

It is essential to stop any tests started from Acuid Tools before invoking the SPD Reader/Writer software. As compensation factors are stored in the DIB SPD here we'll give more consideration to the "DIB" dialog's items.

There are four items in the right part of the "DIB" dialog window:

"Load From File" – allows to load SPD contents from a file.

"Save To File" – allows writing SPD contents into a file.

"Load From Tester" – allows reading SPD of the header submitted to adjustment.

"Save To Tester" – allows writing correction factors into SPD memory. This item is used to complete an iteration of adjustment.

Buttons placed in the left bottom part of the "DIB SPD" dialog window are used to operate with tags in the "Tag" field.

To write correction coefficients into the DIB SPD the following procedure algorithm should be implemented.

1. Select "Load From Tester" item in the "DIB" dialog window.

   Result: tags appear in the "Tags" field.

2. Click "Add" button, then select "Signal Receiver Correction" tag in the "Named tag" field, click "OK".

   Result: the "Signal Receiver Correction" tag is added to the "Tags" field.

If "Signal Receiver Correction" tag is already added to the "Tags" field then it needs to be selected only.

3. Click "Edit" button.

   Result: the "Signal Receiver Correction" window will spawn. Select "bT72_DDR.pin" line in the "Header Pin Set" field. Compensation factors will be shown in the "Compensation" field.

4. Update compensation factors.

To update compensation values, select all signals belonging to the same group, click "Add" button, enter calculated **UPDATE** value to add it to current compensation value. Repeat this for all other groups.

Note that in the signal group "Slot 2" a compensation coefficient should be entered for A14 as well as for all other signals though A14 couldn't be observed with oscilloscope.

"Signal Receiver Correction" dialog window with updated compensation coefficients is shown in figure below.

5. Click "OK" button.

6. Select "Save To Tester" item in the "DIB SPD" dialog window.

7. Close SPD Reader/Writer.

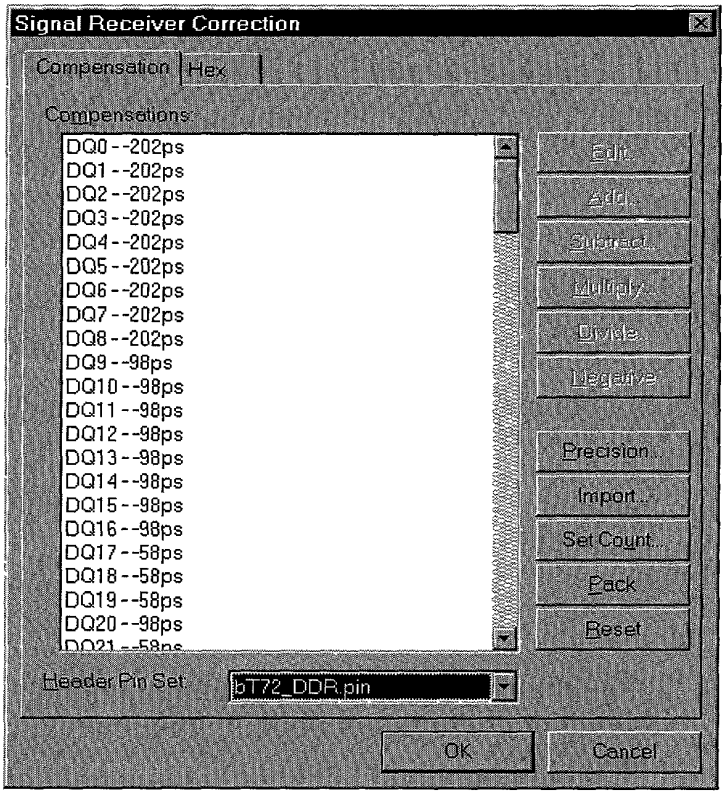


Fig.3. "Signal Receiver Correction" dialog window.

Typical Signal Grouping

The table below provides signal grouping on bT72_DDR Header and an example of a table for skew records.

Slot 1

Signal	DQ4	DQ0	DQ5	DQ1	DQ6	DQ2	DQ7	DQ3	DQ8
R / left									
R / right									
F / left									
F / right									

Slot 2

Signal	A14	A13	BA2	A12	A11	A9	A7	A8	A5
Rising / left									
Rising / right									

Slot 3

Signal	DQ9	DQ12	DQ13	DQ14	DQ15	DQ10	DQ11	DQ20	DQ16
R / left									
R / right									
F / left									
F / right									

Slot 4

Signal	DQ17	DQ21	DQ18	DQ22	DQ19	DQ23	DQ24	DQ28	DQ25
R / left									
R / right									
F / left									
F / right									

Slot 5

Signal	A6	A4	A3	A2	A1	A0	A10	BA1	BA0
Rising / left									
Rising / right									

Slot 6

Signal	DQ29	DQ30	DQ26	DQ27	DQ31	CB4	CB5	CB0	CB1
Rising / left									
Rising / right									
Falling / left									
Falling / right									

Slot 7

Signal	DQS0	DQS1	DQS2	DQS3	DQS8	DQS4	DQS5	DQS6	DQS7
Rising / average									
Falling / average									

Slot 8

Signal	DM0	DM1	DM2	DM3	DM8	DM4	DM5	DM6	DM7
Rising / left									
Rising / right									
Falling / left									
Falling / right									

Slot 9

Signal	CK1	CK0	CK2
Rising / average			
Falling / average			

Slot 10

Signal	CB2	CB6	CB3	CB7	DQ32	DQ36	DQ33	DQ37	DQ34
Rising / left									
Rising / right									
Falling / left									
Falling / right									

Slot 11

Signal				CKE1	CKE0	RAS	WE	CAS	FETEN
Rising / left									
Rising / right									

Slot 12

Signal	DQ38	DQ39	DQ35	DQ40	DQ44	DQ45	DQ41	DQ42	DQ43
Rising / left									
Rising / right									
Falling / left									
Falling / right									

Slot 13

Signal	S0	S1	S2	S3
Rising / left				
Rising / right				

Slot 14

Signal	DQ46	DQ47	DQ48	DQ49	DQ52	DQ53	DQ54	DQ55	DQ50
Rising / left									
Rising / right									
Falling / left									
Falling / right									

Slot 15

Signal	DQ51	DQ60	DQ61	DQ56	DQ57	DQ62	DQ63	DQ58	DQ59
Rising / left									
Rising / right									
Falling / left									
Falling / right									